Google

Advanced Search Preferences Language Tools Search Tips

circuit simulation "hierarchical analysis"

Google Search

Web Images Groups Directory

Searched the web for circuit simulation "hierarchical analysis". Results 1 - 100 of about 142. Search took 0.

Mach - **Circuit Simulation** for Timing and Power Analysis
... manage large extracted netlists through **circuit simulation**. • Accelerate your SPICE simulations from 30X to 1,000X. • See our new **Hierarchical Analysis**, ...
www.mentor.com/mach/mach_wksp.html - 29k - Cached - Similar pages

IC deep submicron accelerated **simulation** and timing analysis: ...
... with Machcal, which then invokes your preferred **circuit** ... HA to Mach TA that supports **Hierarchical Analysis** ...
www.mentor.com/mach/qa.html - 29k - Cached - Similar pages
[More results from www.mentor.com]

Research project: **Hierarchical analysis**
Hierarchical Analysis. Short description. ... Especially, algorithms suitable for **circuit simulation** in networks of workstations (NOW) will be developed. ...
www.aplac.hut.fi/research/hierarchical.html - 3k - Cached - Similar pages

HUT/CT-lab/research activities
... Steady-state analysis methods (1993-); Electrothermal **circuit simulation** ... 1994-); Mixed-mode analog digital **simulation** (1997-); **Hierarchical analysis** ...
www.aplac.hut.fi/research/main.html - 4k - Cached - Similar pages
[More results from www.aplac.hut.fi]

Wlodek M. Zuberek's Home Page
... 34-th Annual **Simulation** Symposium (SS-2001), Seattle, WA, pp.93-98, April 2001. "**Hierarchical analysis** of manufacturing systems using Petri nets"; Proc. ...
web.cs.mun.ca/~wlodek/ - 9k - Cached - Similar pages

DSM Interconnect Modeling and Analysis for Performance and ...
... analysis concepts and requirements: **hierarchical analysis**; monotone ... switching, internal state, cycles in **circuit** ... **simulation**-based; probabilistic. standard power ...
asic.union.edu/Asic98/Wrkshp/submicron.prop.html - 8k - Cached - Similar pages

[PDF] HSIM
File Format: PDF/Adobe Acrobat - View as HTML
... By combining this with a **hierarchical analysis**, HSIM ... thousand transistors which have extremely long **simulation** ... can now be simulated successfully at the **circuit** ...
www.nassda.com/HSIMbrochure21.pdf - Similar pages

Synopsys RailMill -- Datasheet {2172.001}
... Integrated Analog **Circuit** Engine (ACE) for mixed signal circuits; Dynamic **simulation** with ... PNA) Footprint technology enables full chip **hierarchical analysis** ...
www.synopsys.com/products/phy_syn/railmill_ds.html - 14k - Cached - Similar pages

[PDF] RailMill DS-A4web
File Format: PDF/Adobe Acrobat - View as HTML

... critical **circuit** blocks - Integrated Analog **Circuit** ... for mixed signal circuits - Dynamic **simulation** ... Footprint technology enables full chip **hierarchical analysis** ...
www.synopsys.com/products/phy_syn/railmill_ds_A4.pdf - Similar pages
[More results from www.synopsys.com]

Computer Aids for VLSI Design
... Race Analysis of Digital Systems Without Logic **Simulation**," ... Hon, Robert W., The **Hierarchical Analysis** of VLSI ... Artwork Verification Program for Printed **Circuit** ...
www.rulabinsky.com/cavd/text/chap05-6.html - 11k - Cached - Similar pages

Computer Aids for VLSI Design
... [8]; Hon, Robert W., The **Hierarchical Analysis** of VLSI Designs, PhD ... [4]; Wang, Paul KU, "Approaches to Hardware Acceleration of **Circuit Simulation**," Proceedings ...
www.rulabinsky.com/cavd/text/chapf.html - 47k - Cached - Similar pages

IEEE Transactions on Computer-Aided Design of Integrated Circuits ...
... (2112); Min Zhao, Rajendra Panda, Sachin Sapatnekar, David Blaauw, **Hierarchical Analysis** of ... Table Look-Up Model of Thin-Film Transistors for **Circuit Simulation** ...
tcad.ece.orst.edu/list02.html - 16k - Cached - Similar pages

Citations: Computer Methods for **Circuit** Analysis and Design - ...
... to **circuit simulation** and overviews of typical **simulation** ... Vlach and K. Singhal, Computer Methods for **Circuit** ... 2. OVERVIEW OF **HIERARCHICAL ANALYSIS** BY SUBCIRCUIT ...
citeseer.nj.nec.com/context/58212/0 - 34k - Cached - Similar pages

Untitled
Papers on Analog **Simulation** JA Starzyk, "Topological ... Journal of **Circuit** Theory and Applications, Vol. ... JA Starzyk, "**Hierarchical Analysis** of High Frequency ...
www.ent.ohiou.edu/~starzyk/network/ Research/AnalogPapers.html - 8k - Cached - Similar pages

Year Sponsor Topic Amount 1984 Valid Logic Inc. Equipment Grant ...
... LLS Networks by Means of Upward **Hierarchical Analysis**", ... Signal Testing of Analog Components on Printed **Circuit** ... JA Starzyk, and YW Jan," A **Simulation** Program ...
www.ent.ohiou.edu/~starzyk/network/resume2000.htm - 44k - Cached - Similar pages

Artes
... This is the so-called **hierarchical analysis**. ... SMV models a system eg a hardware **circuit** as a ... supports two-level hierarchy; but SDT is basically a **simulation** tool ...
www.artes.uu.se/project/9811-5/ - 11k - Cached - Similar pages

IEEE Transactions on Computer-Aided Design of Integrated Circuits ...
... Panda, Sachin Sapatnekar, David Blaauw, **Hierarchical Analysis** of ... Cheng, and Cheng-Wen Wu, Fault **Simulation** ... Walter Daems, Georges Gielen, Willy Sansen, **Circuit** ...
akebono.stanford.edu/users/nanni/tcad/list02.html - 9k - Cached - Similar pages

MONARCH Research Overview
... language VHDL-AMS in order to develop a **hierarchical analysis** capability which will cover both architectural system **simulation** and individual **circuit** component ...
www.ee.duke.edu/research/MONARCH/overview.html - 4k - Cached - Similar pages

[PDF] **Hierarchical Analysis** of Power Distribution Networks
File Format: PDF/Adobe Acrobat - View as HTML
... In this paper, we propose a **hierarchical analysis** ... is circumvented traditionally [1] by per- forming nonlinear **simulation** of individual **circuit** ...
www.sigda.org/Archives/ProceedingArchives/Dac/ Dac2000/papers/2000/dac00/pdffiles/09_1.pdf - Similar pages

DAC 2000 Table of Contents
... Organizers: Ingrid Verbauwhede, Mojy Chian 9.1 **Hierarchical Analysis** of ... p. 150] 9.2 Fast Power Grid **Simulation** ... Die Interconnect and Device Variation on **Circuit** ...
www.sigda.org/Archives/ProceedingArchives/Dac/Dac2000/papers/2000/dac00/htmfiles/sun_sgi/dactoc.htm - 64k - Cached - Similar pages
[More results from www.sigda.org]

Cover Story - February 1997
... to develop a new methodology based on **hierarchical analysis** ... of reasons: PathMill analyzes high-performance **circuit** ... reduces the amount of data for **simulation**. ...
www.eedesign.com/editorial/1997/coverstory9702.html - 41k - Cached - Similar pages

InterHDL offers RTL planning tools
... over half of the problems you'd find in **simulation** ... The first new offering, Checkit, is a **hierarchical analysis** ... domains, which are portions of a digital **circuit** ...
www.eetimes.com/dac98/news_offers.html - 19k - Cached - Similar pages

Homepage Francky Leyn
... Techniques that were investigated include symbolic **simulation**, ... Given a certain **circuit** description the ... be used as bookkeeping system for **hierarchical analysis**, ...
www.esat.kuleuven.ac.be/~leyn/ - 28k - Cached - Similar pages

[PDF] An assessment of the technological needs for a competence-based, ...
File Format: PDF/Adobe Acrobat - View as HTML
... Briefly, the methodology starts with a top-down **hierarchical analysis** of learning ... complementary type of tool had to be used together with **circuit simulation** ...
www.ehis.navy.mil/tp/humanscience/papers/art24.pdf - Similar pages

[DOC] Eurogram 97-4
File Format: Microsoft Word 6 - View as HTML
... data structure for object fitting **hierarchical analysis** ... include Experimental and Numerical Vortex **Simulation**, ... however, the department also researches **circuit** ...
www.ehis.navy.mil/eurogram/julaug97/julaug97.doc - Similar pages

Abstract1
... in Symbolic **Circuit** Analysis. **Circuit simulation** ... if required, numerical responses of the **circuit**. ... based (topological) or matrix approach, **hierarchical analysis**, ...
www.eng.uts.edu.au/~jafarm/Seminar2001/Abstract1.htm - 22k - Cached - Similar pages

[PDF] Modeling and **Simulation**
File Format: PDF/Adobe Acrobat - View as HTML
... By using these algorithms in a **hierarchical analysis**, we expect ... extensions supporting hierarchical designs and utilizing higher performance **circuit simulation** ...
www-mtl.mit.edu/mtlhome/6Res/AR1999/AR99-MS.pdf - Similar pages

[PDF] Fast Analysis and Optimization of Power/Ground Networks Abstract ...
File Format: PDF/Adobe Acrobat - View as HTML
... current across the same element in the adjoint **circuit**, ... 2. **Hierarchical analysis** of the P/G network ... The **simulation** is event-driven, proceeding one interval ...
www.ece.umn.edu/users/sachin/PUBS/iccad00b.pdf - Similar pages

Defect-Based Test: A Key Enabler for Successful Migration to ...
... can be applied to the problem: **Hierarchical analysis**. ... that are robust (less susceptible to off-path **circuit** ... to simplifying the model to ease fault **simulation** ...
www.intel.com/technology/itj/ q11999/articles/art_6g.htm - 22k - Cached - Similar pages

[PDF] Defect-Based Test: A Key Enabler for Successful Migration to ...
File Format: PDF/Adobe Acrobat - View as HTML
... However, due to the number of possible defect sites and the complexity of **circuit simulation**, this can only be done for a small sample. ...
www.intel.com/technology/itj/ q11999/pdf/defect_based.pdf - Similar pages

[PDF] Efficient Large-Scale Power Grid Analysis Based on Preconditioned ...
File Format: PDF/Adobe Acrobat - View as HTML
... for DC analysis and around 10 times faster for transient **simulation** ... A robust power network design has to guarantee the correctness of **circuit** ...
vlsi.ece.wisc.edu/research/2001dac01.pdf - Similar pages

[PS] vlsi.ece.wisc.edu/research/hmor.ps
File Format: Adobe PostScript - View as Text
... and theoretical foundations to facilitate the **hierarchical analysis**. ... LT Pillage, RA Rohrer, C. Visweswariah, Electronic. **Circuit** and System **Simulation** ...
Similar pages

HICSS: Table of Contents
... A **Hierarchical Analysis** Approach for High Performance ... in the Deregulated Energy Market through **Simulation** ... Dynamic **Circuit** Generation for Boolean Satisfiability ...
www.computer.org/proceedings/ hicss/0001/00013/0001toc.htm - 33k - Cached - Similar pages

[PS] www.imse.cnm.csic.es/online/1996/imse96_004.ps.gz
File Format: Adobe PostScript - View as Text
... solution has been shownto be the application of **hierarchical analysis** ... **Circuit** Theoryand Design, pp. ... and PM Lin, "A New Network Approach toSymbolic **Simulation** ...
Similar pages

Silvaco
... SPICE format used for running external LVS programs and **circuit simulation**. ... References. [1] LK Scheffer, R. Soetarman "**Hierarchical Analysis** of IC Artwork", Proc ...
www.silvaco.com/applications/archive/ june_98/a1/jun98_a1.html - 47k - Cached - Similar pages

[PDF] Deep-Submicron Issues in High-Performance Design
File Format: PDF/Adobe Acrobat - View as HTML
... of the **circuit** to low Vt, overall **circuit** ... power estimation or detailed transistor-level **simulation**. ... 3. Post-Layout IR-drop Analysis This **hierarchical analysis** ...
patmos2001.eivd.ch/program/Repro%5CArt_5_1.pdf - Similar pages

Untitled
... Optimization through Threshold Voltage Selection and **Circuit** ... Edwards, Rajat Chaudhry, David Blaauw, ``**Hierarchical Analysis** ... and On-Chip Power Grid **Simulation**," ...
www.eecs.umich.edu/~blaauw/pubs.html - 4k - Cached - Similar pages

[PDF] Electrical integrity design and verification for digital and ...
File Format: PDF/Adobe Acrobat - View as HTML
... November 8, 2001 ICCAD 2001 Design methodology for noise for digital circuits * Dynamic **simulation** ... listener - very hard to generalize to different **circuit** ...
www.eecs.umich.edu/~dennis/ICCAD01.pdf - Similar pages
[More results from www.eecs.umich.edu]

[PDF] Multi-Agent **Simulation** and Educational Tool for Power System ...
File Format: PDF/Adobe Acrobat - View as HTML
... the best strategy to reclose switches, and **circuit** ... and design of a educational and **simulation** ... And more, it gives possibility to includes **hierarchical analysis** ...
www.asee.org/international/INTERTECH2002/178.pdf - Similar pages

37. Design Automation Conference
... S. Sapatnekar, Tim Edwards, Rajat Chaudhry, David Blaauw: **Hierarchical analysis** ... Chebyshev collocation method for efficient high-accuracy RF **circuit simulation**. ...
www.informatik.uni-trier.de/~ley/ db/conf/dac/dac2000.html - 85k - Cached - Similar pages

HICSS 1999
... Zhou, Haibo Xu, Shihab Ghaya: A **Hierarchical Analysis** ... in the Deregulated Energy Market through **Simulation**. ... DL); Oskar Mencer, Marco Platzner: Dynamic **Circuit** ...
www.informatik.uni-trier.de/~ley/ db/conf/hicss/hicss1999-3.html - 33k - Cached - Similar pages

[PDF] Who Has Nanometer Design Under Control?
File Format: PDF/Adobe Acrobat - View as HTML
... in victim Logic 0 in victim Solid 0 Real **circuit** on silicon What existing ... o Detailed **simulation** may find some noise problems, but it will be ineffective ...
videos.dac.com/videos/38th/36/36/36slides.pdf - Similar pages

tas.1
... an accuracy better than 10% versus SPICE **simulation**. ... out a flattened timing view of the **circuit** and ... In the **hierarchical analysis** mode, tas uses existing timing ...
www-asim.lip6.fr/alliance/doc/man/tas.1.html - 31k - Cached - Similar pages

[PDF] Multigrid-like Technique for Power Grid Analysis
File Format: PDF/Adobe Acrobat - View as HTML
... Checking the integrity of the supply voltage using traditional **circuit simulation** is not practi- cal, for reasons of time and memory complexity. ...
www.eecg.toronto.edu/~najm/papers/iccad01-kozhaya.pdf - Similar pages

[PS] www.eecg.toronto.edu/~najm/papers/iccad01-kozhaya.ps
File Format: Adobe PostScript - View as Text
... Fast power grid **simulation**. ... al. **Hierarchical analysis** of power distribution networks. ... Interconnect
and **circuit** modeling. techniques for full-chip power noise ...
Similar pages

Nat'l Academy Press, Large-Scale Structures in Acoustics and ...
... frequency, modeling, block, figure, parameter, line, model, **simulation**, **circuit**, ... transmission, array, fabrication, diagram, wave, integrated, **hierarchical**, **analysis**, ...
www.nap.edu/books/0309053374/html/143.html - 58k - Cached - Similar pages

OSU-CITR Report Series
... mechanical motion equations and the hydraulic **circuit** ... to immerse themselves in a **simulation** ... illustrate this methodology, we describe the **hierarchical analysis** ...
eewww.eng.ohio-state.edu/citr/report.html - 28k - Cached - Similar pages

iordache
... Nonlinear electric and electronic circuits (computer-**simulation**, ... or/and nonlinear circuits; **Hierarchical analysis** ... Large-Scale Electric and Electronic **Circuit** ...
www.elth.pub.ro/fara/pop/iordache/iordache.html - 5k - Cached - Similar pages

[PDF] Harmony: static noise analysis of deep submicron digital ...
File Format: PDF/Adobe Acrobat - View as HTML
... This creates a clean partitioning between one CCC and the next and is a technique commonly employed in fast **circuit simulation** engines [19]. ...
www.cisl.columbia.edu/faculty/shepard/ publications/harmony.pdf - Similar pages

Publications: Integrating CBI Approaches into Simulator Training ...
... a classic four-level task and skills **hierarchical analysis** ... All PCs designated for 3D **simulation**, taken as a group ... activities of personnel as diverse as **circuit** ...
www.agentwaresystems.com/Publications/media.htm - 43k - Cached - Similar pages

[PDF] Mentor Graphics' 1998 Product Portfolio
File Format: PDF/Adobe Acrobat - View as HTML
... supports existing V-System and QuickHDL **simulation** ... Complete design rule checking (DRC), **circuit** ... achieve new levels of performance with **hierarchical analysis**. ...
www.te.rl.ac.uk/europractice/vendors/mentor.pdf - Similar pages

[PS] www.te.rl.ac.uk/europractice/vendors/mentor.ps
File Format: Adobe PostScript - View as Text
... new levels of performancewith **hierarchical analysis**. ... can be saved, incrementallyrecompiled, and the **simulation** ... a comprehensive environment for printed **circuit** ...
Similar pages

Plenary Talks, Symposia and Workshop in ICCS99
... is used in the **circuit** ... The **simulation** replicated the results of ... 50; Speaker: ? ????? ???????????; Title: **Hierarchical Analysis** ...
www.sccs.chukyo-u.ac.jp/ICCS99/plenary-talks-jpn.html - 38k - Cached - Similar pages

Plenary Talks, Symposia and Workshop in ICCS99
... based representation is used in the **circuit** ... The **simulation** replicated the results of sequence ... of Science, Osaka City University; Title: **Hierarchical analysis** of ...
www.sccs.chukyo-u.ac.jp/ICCS99/plenary-talks.html - 39k - Cached - Similar pages
[More results from www.sccs.chukyo-u.ac.jp]

[PDF] 44 IEEE Midwest Symposium on Circuits and Systems
File Format: PDF/Adobe Acrobat - View as HTML
... ANALOG NEURON **CIRCUIT** DESIGN, ANALYSIS, AND **SIMULATION**. ... SYSTEM USING MIXED-MODE CHAOTIC
CIRCUIT. ... OF LOGIC INTEGRATED SYSTEMS BASED ON **HIERARCHICAL ANALYSIS**. ...
www.ececs.uc.edu/~hcarter/mwscas/conference-public/ final_program.pdf - Similar pages

hawk.ise.chuo-u.ac.jp/NOLTA/95/ad-pro.txt
... from Session 7B) [8C] Chaotic Series Analysis [8D] **Circuit Simulation** and ... Akifumi, TAKAKUBO, Hajime, SHONO, Katsufusa (Sophia Univ.) ``A **Hierarchical Analysis** ...
53k - Cached - Similar pages

NOLTA'95 Final Program
... from Session 7B) [8C] Chaotic Series Analysis [8D] **Circuit Simulation** and ... Akifumi, TAKAKUBO, Hajime, SHONO, Katsufusa (Sophia Univ.); ``A **Hierarchical Analysis** ...
hawk.ise.chuo-u.ac.jp/NOLTA/95/ad-pro.html - 55k - Cached - Similar pages
[More results from hawk.ise.chuo-u.ac.jp]

Keyword Index
... asynchronous **circuit** (4 entries); asynchronous **circuit** ... semantics (2 entries); exhaustive **simulation** (2 ... 4 entries); hierarchical (2 entries); **hierarchical analysis** ...
www.informatik.uni-hamburg.de/TGI/pnbib/keywords/ - 101k - Cached - Similar pages

DATE 2000 Programme
... The third paper combines layout synthesis and **circuit** ... 15.30, VIRTUAL FAULT **SIMULATION** OF DISTRIBUTED IP ... the complications of DSP cores and **hierarchical analysis**. ...
www.c-lab.de/~date/programme2000.html - 101k - Cached - Similar pages

Design, Automation and Test in Europe
... This paper introduces a new **hierarchical analysis** methodology ... to predict such error rates straightforward, **simulation** ... The analyzed **circuit** is modeled as finite ...
www.date-conference.com/conference/2000/abstracts.htm - 101k - Cached - Similar pages

Why2K Proposal
... the task domain was a ?black box expert,? namely, a **circuit simulation** ... Technologies based on compositional semantics often build a **hierarchical analysis** of ...
mnemosyne.csl.psyc.memphis.edu/onr/MURI/proposal.htm - 101k - Cached - Similar pages

[DOC] Why2K Proposal
File Format: Microsoft Word 2000 - View as HTML
... the task domain was a "black box expert," namely, a **circuit simulation** ... Technologies based on compositional semantics often build a **hierarchical analysis** of ...
mnemosyne.csl.psyc.memphis.edu/onr/MURI/proposal.doc - Similar pages

BIOMEDICAL ENGINEERING
... **Circuit** and structure analysis for conditioning signals. ... 8. EMC **Simulation** tools. ... Cluster analysis with distance and closeness measures, **hierarchical analysis** ...
www.upc.es/tercercicle/Eng/Doctorat/Programes/25.htm - 78k - Cached - Similar pages

Abstracts for Robert K. Brayton
... the control and a special form of symbolic **simulation** ... times at primary inputs of the entire **circuit** ... is the first result that shows that **hierarchical analysis** ...
buffy.eecs.berkeley.edu/IRO/Summary/ 98abstracts/abstracts.RKB.html - 34k - Cached - Similar pages

Computer-Aided Design for 1998
... is the first result that shows that **hierarchical analysis** ... and to thus serve as an indispensable **circuit** ... To address the need for comparably efficient **simulation** ...
buffy.eecs.berkeley.edu/IRO/Summary/ 98abstracts/chapter1.html - 101k - Cached - Similar pages

Archeology and Cognitive Science
... (b) The **circuit** level consists of ... the evaluation of similar phenomena, computer **simulation**, ... a computational system that incorporates a **hierarchical analysis** of ...
cas-courses.buffalo.edu/classes/psy/segal/ARCHCHAP.htm - 47k - Cached - Similar pages

[PDF] Page 1
File Format: PDF/Adobe Acrobat - View as HTML
Page 1. ... which may or may not be detectable, and some can make the **circuit** ... the DUDES fault model is to significantly reduce the complexity of fault **simulation**, ...
research.sun.com/async/Publications/KPDisclosed/ sml2000-0057/csml2000-0057.pdf - Similar pages

[PDF] PIECEWISE LINEAR MODELING AND ANALYSIS
File Format: PDF/Adobe Acrobat - View as HTML
... to analyze a **circuit** behavior certainly when the **circuit** ... Aspects as DC, AC and transient **simulation** will ... bias point and how to perform a **hierarchical analysis**. ...
www.mea.isim.univ-montp2.fr/POLYCOPS/ divers/syst_non_lin:Van_Bokhoven.pdf - Similar pages

[PS] www.ece.purdue.edu/~chengkok/papers/ispd01_decap.ps
File Format: Adobe PostScript - View as Text
... **Simulation** and optimization of the power distribution network ... International Journal of **Circuit** Theory and ... **Hierarchical analysis** of power distribution. networks. ...
Similar pages

[PS] www.ece.purdue.edu/~chengkok/papers/tcad02_decap.ps
File Format: Adobe PostScript - View as Text

... **Simulation** must be performed to identify the ... decoupling capacitance budget by judiciously arranging **circuit** ... R. Chaudhry, and D. Blaauw, "**Hierarchical analysis** ...
Similar pages

Untitled Document
... applicable for other types of analysis and **simulation**, ... Tree Analysis - a top-down, **hierarchical analysis** of ... provides complete access to an integrated **circuit**. ...
members.aol.com/drmassoc/glossary.html - 83k - Cached - Similar pages

ICRA02 Accepted Papers
... Continuous-Time Impedance Display by Analog **Circuit**, ... 594, Dynamic **simulation** of a Humanoid robot ... 810, **Hierarchical Analysis** For Determining Disconnectedness in a ...
www.icra-iros.com/icra2002/accepted.html - 101k - Cached - Similar pages

[PDF] Tuesday, June 6
File Format: PDF/Adobe Acrobat - View as HTML
... Thursday, June 3 BREAK Interconnect Analysis High ... Applications Embedded Tutorial: MOSFET Modeling and **Circuit** ... Advances in High Level Synthesis Fault **Simulation** ...
www.dac.com/39th/PDFs/37glance.pdf - Similar pages

[PDF] Analysis and Optimization of Object Systems
File Format: PDF/Adobe Acrobat
... following sections. It would be possible to gain class membership information by profiling model execution (**simulation**), too. However ...
docserver.bis.uni-oldenburg.de/publikationen/ dissertation/2000/radsyn00/pdf/chap06.pdf - Similar pages

EDN Access--12.04.97 Leading Edge
... than 1 µA. In addition to short-**circuit**, ... on-chip timing paths without the use of **simulation** ... In addition, a linear-analysis algorithm and **hierarchical analysis** ...
archives.e-insite.net/archives/ednmag/ reg/1997/120497/25le.htm - 47k - Cached - Similar pages

NEW PRODUCT DEVELOPMENT GLOSSARY
... CAT, Computer-Aided Test. CCA, **Circuit** Card Assembly. ... of electronic products through design capture, **simulation**, ... Tree Analysis is a top-down, **hierarchical analysis** ...
www.npd-solutions.com/glossary.html - 101k - Cached - Similar pages

[PDF] Efficient Power Estimation for Highly Correlated Input Streams
File Format: PDF/Adobe Acrobat - View as HTML
... continuing throughout the **circuit**. Recently, a few approaches which account for correlations have been proposed: using an event-driven probabilistic **simulation** ...
cselab.snu.ac.kr/course/csd99/paper/2_20.pdf - Similar pages

[PS] www.ece.arizona.edu/~hpdc/publications/net_hpcc.ps
File Format: Adobe PostScript - View as Text
... this problem and develop aconvenient **hierarchical analysis** ... there are several existing network modelingand **simulation** ... which is applied to electrical **circuit** ...
Similar pages

????
... [57] Murata, T., ?**Circuit** Theoretic Analysis and Synthesis of Marked Graphs ...
[77] Valvanis, KS, ?On the **Hierarchical Analysis** and **Simulation** of. ...
www.mis.nccu.edu.tw/demo/paperlist/89/86(30).htm - 48k - Cached - Similar pages

1. Introduction
... was achieved by using in-house **hierarchical analysis** ... JL, "Application Specific CMOS

Output Driver **Circuit** ... Sang Soo Lee, Allstot D., "Electrothermal **Simulation** ...
vlsi.wpi.edu/webcourse/digittv/digittv.html - 57k - Cached - Similar pages

DATE 2000 Abstracts
... This paper introduces a new **hierarchical analysis** methodology ... current properties per terminal gained by **simulation** or manually specified by **circuit** ...
www.edatoolscafe.com/.../ProceedingArchives/Date/Date2000/papers/2000/date00/htmfiles/sun_sgi/dateabs.htm - 101k - Cached - Similar pages

[PS] www-cad.eecs.berkeley.edu/~kenmcmil/pubs/TCAD91.ps.gz
File Format: Adobe PostScript - View as Text
... state model from section 4 which can be used in a **hierarchical analysis** ... with an analog transistor **circuit** model, similar to models used in **circuit simulation**, ...
Similar pages

High-level description languages, HDLs and SoC information for IC ...
... ASIC Libraries (Vital) modeling specification for VHDL **simulation** ... an in-depth flat or **hierarchical analysis** of a transistor netlist in Spice or CDL (**circuit**- ...
www.chipcenter.com/hdl/main_4.html - 37k - Cached - Similar pages

[PS] www.cs.cmu.edu/~bryant/pubdir/tcad87b.ps
File Format: Adobe PostScript - View as Text
... This **hierarchical analysis** would require less time and ... Race Detection in MOS Circuits by Ternary **Simulation**", ... Takashima, et al, "Programs for Verifying **Circuit** ...
Similar pages

ESNUG Post 375
... use it to replace the RTL block in **simulation**, or ... This combination allows me to do **hierarchical analysis** at ... events, which represents a benefit for ANY **circuit** ...
www.paume.itb.ac.id/rahard/esnug/msg00157.html - 53k - Cached - Similar pages

www.research.ibm.com/journal/rd/414/shepard.txt
... result, the approach we take is an essentially two-level **hierarchical analysis** ... We perform the macro **circuit simulation** using the SPECS (**Simulation** Program for ...
101k - Cached - Similar pages

[PDF] INSTITUTO DE TELECOMUNICAÇÕES Relatório Anual 1996
File Format: PDF/Adobe Acrobat
Page 1. INSTITUTO DE TELECOMUNICAÇÕES Relatório Anual 1996 Page 2. 2 INDICE 1. INTRODUÇÃO ...
www.it.pt/anuais/rep96.pdf - Similar pages

[PDF] INSTITUTO DE TELECOMUNICAÇÕES Relatório de Actividades 1998
File Format: PDF/Adobe Acrobat
Page 1. INSTITUTO DE TELECOMUNICAÇÕES Relatório de Actividades 1998 Page 2. Relatório de Actividades - 1998 2 Page 3. Relatório ...
www.it.pt/anuais/rep98.pdf - Similar pages
[More results from www.it.pt]

SPIE Proceedings Vol. 3392
... Paper #: 3392-98) * Bayesian **hierarchical analysis** of ... performance, measured through Monte Carlo **simulation** ... tool monitoring, medical prediction, digital **circuit** ...
www.spie.org/web/abstracts/3300/3392.html - 101k - Cached - Similar pages

SPIE Proceedings Vol. 2727c
... The overall coarse-to-fine **hierarchical analysis** and ... The **simulation** results indicate

that our algorithm shows ... We discuss an analog VLSI **circuit** implementation ...
www.spie.org/web/abstracts/2700/2727c.html - 57k - Cached - Similar pages
[More results from www.spie.org]

[PDF] System Sciences
File Format: PDF/Adobe Acrobat - View as HTML
... Work Environments Electronic Commerce Technologies Mobile Computing Modern Cluster Computing Multimedia DBMS and WWW Parallel and Distributed **Simulation** ...
www.cit.uws.edu.au/pub/doc/cit/hiccs32/hicss32.pdf - Similar pages

[PDF] Commercial in Confidence
File Format: PDF/Adobe Acrobat - View as HTML
... It modifies a user-specified unit in order to simulate errors in the code and runs a **simulation** in which the user code is simulated in parallel with the error ...
www.upmdie.upm.es/~ardid/prog/ArdidUserGuide.pdf - Similar pages

[PDF] N 3067 N 556
File Format: PDF/Adobe Acrobat - View as HTML
Page 1. Secretariat ISO/IEC JTC ... 19 5.12 Model orientated procedure with **hierarchical analysis** ... 53 5.83 Sneak **circuit** analysis ...
www.gammassl.co.uk/ist33/27n3067.pdf - Similar pages

[DOC] Second Announcement
File Format: Microsoft Word 2000 - View as HTML
... sequence in knowledge possessed with deduction and logic; the research habit of analyzing real-world problems and mathematical modeling and computer **simulation** ...
csiam.edu.cn/ictma10/ictma10Last.doc - Similar pages

[PDF] Functional and Diagrammatic Representation for Device Libraries
File Format: PDF/Adobe Acrobat - View as HTML
... and criticism * Technology for automatically extracting monitoring and diagnostic knowledge from design representations * Technology for composable **simulation** ...
www.cis.ohio-state.edu/lair/Projects/ MADE/annual-report-98.PDF - Similar pages

[PDF] Subject Categories of the Division H. Physics
File Format: PDF/Adobe Acrobat - View as HTML
... A delay storage **circuit** includes time delays for each projector for each of ... modeling has advanced in the past few years allowing better **simulation** of ...
www.sti.nasa.gov/Pubs/star/9617/divh.pdf - Similar pages

[RTF] INSTITUTO DE TELECOMUNICAÇÕES
File Format: Rich Text Format - View as HTML
... E. Franca), Instituto Superior Técnico, in preparation, (subject: Analog **circuit** ... It deals with the **hierarchical analysis** of the microstructure of sleep ...
www.lx.it.pt/relatorio97.rtf - Similar pages

[PS] home.attbi.com/~kukimoto/thesis.ps.gz
File Format: Adobe PostScript - View as Text
... The **hierarchical analysis** gives as a byproduct incremental analysis capability, which is ... **Circuit simulation** such as SPICE directly solves a set of differential ...
Similar pages

[PDF] Simulating Tutors with Natural Dialog and Pedagogical Strategies
File Format: PDF/Adobe Acrobat - View as HTML
... the task domain was a "black box expert," namely, a **circuit simulation** ... Technologies based on compositional semantics often build a **hierarchical analysis** of the ...

www.rhodes.edu/lltlab/Person/ publications/TenureMURI.pdf - Similar pages

[PDF] JOURNAL ARTICLE
File Format: PDF/Adobe Acrobat - View as HTML
Page 1. IA Report (Squash) Annex G.doc 1 19/05/02 20:49 Annex G Report of the Sub-Committee on Stock Assessment - In Depth Assessments ...
www.iwcoffice.org/SCWEB/SCRepFiles2002/AnnexG.pdf - Similar pages

Google ▶
Result Page: 1 2 **Next**

circuit simulation "hierarchical analysis" Google Search Search within results

Dissatisfied with your results? Help us improve.

Try your query on: AltaVista Excite Lycos Yahoo!

Google Home - Advertise with Us - Search Solutions - News and Resources - Language Tools - Jobs, Press, Cool Stuff...

June 30, 2002

System Design

Timing Analysis for the PA-8000

HP engineers developed two timing analysis methodologies to optimize the PA-8000 microprocessor.

by Clay McDonald, Tom Indermaur, and Mike Buckley

This article by Clay McDonald, Tom Indermaur, and Mike Buckley is the second in a series of three that describe the design of Hewlett-Packard's PA-8000 microprocessor--the heart of the company's latest generation workstations. The first appeared in our January 1997 issue. The third will run in the March 1997 issue. The three articles are extracted from presentations being made at Design Supercon97 (Santa Clara, CA) this month.

As metal line widths decrease and transistor counts increase, timing verification of state-of-the-art microprocessors becomes both more critical and more challenging. RC delay, once a second-order effect, now dominates global signal budgets and requires highly detailed analyses. At the same time, chip complexity continues to grow, increasing capacity and data management requirements. To meet these challenges for the PA-8000 microprocessor, the CPU and tool development teams at Hewlett-Packard Co. (Fort Collins, CO) developed two global timing analysis methodologies excelling in accuracy, completeness, and flexibility.

Our early global timing methodology addressed only global interconnect analysis, generating feedback to improve routing, floorplanning, and global signal timing and budgeting. These processes performed well and enabled us to achieve a high confidence level in our global timing

design before silicon was available.

Most importantly, the PA-8000 met the target frequency of 180 MHz with margin on first silicon. In addition, the timing model accurately predicted many critical paths later observed and measured on silicon.

At first tape release, we set out to develop a new methodology to provide greater accuracy, detail, and visibility. Our goal was to aid silicon characterization of the PA-8000 as well as devise a new methodology for future development projects.

This second methodology was successful in producing greater verification coverage and model accuracy, and played a key role in ensuring delivery of a high-quality PA-8000 design to our customers.

The design The PA-8000 is an extremely large and complex full-custom design, containing 3.8 million logic transistors. Fabricated using a 0.5-µm technology with five layers of metal, it operates at 180 MHz and issues instructions out of a 56-entry reorder buffer to achieve leading-edge performance.

RC challenges The PA-8000's size and complexity required a hierarchical design approach. At the top level of the design hierarchy, approximately 6,000 global routed signals are devoted to interconnected communication between the various functional units. The task of modeling all the interconnect, as well as the full custom circuitry employed, presented a great challenge.

Interconnect resistance is a complicating factor in timing analysis. Additional nodes must be defined to describe the R and C element interconnections. The resulting volume of data can quickly overwhelm a computer's resources. In addition, RC nets are often split across hierarchy, introducing a wealth of corner cases and modeling issues. Guaranteeing correct connectivity of the complex RC networks in an evolving design presents more difficulties.

listing of reports from the conference, as well as a listing of significant product announcements made in the month leading up to DAC. Check it out to make sure you haven't missed anything.

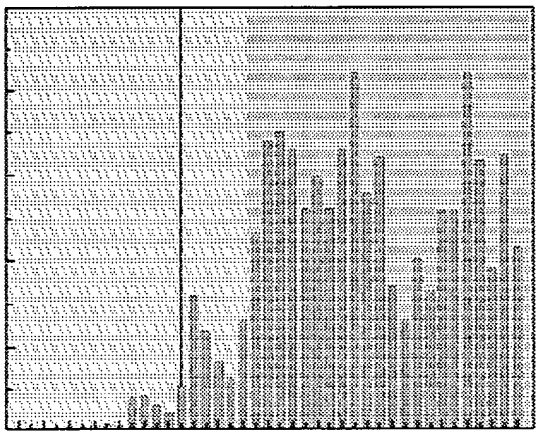
ISD endures, too
While the June 2002 issue was the last for Integrated System Design (ISD) magazine, we'll still maintain our ISD archive site. Here you'll find a provocative June cover story, in which Agere Systems' Bryan Ackland calls on EDA vendors to support a correct by construction design methodology.

Cadence users, unite
The International Cadence User's Group is holding its annual conference in San Jose, Calif., Sept. 16-18. You can register now at the group's web site. You will find this user's group, and others, listed on our left navbar under "Industry Groups."

Finding the "wall"

One of the most useful outcomes of a global timing analysis is finding the "wall." This is the point of diminishing returns--the point beyond which pushing the frequency by fixing speed paths becomes increasingly difficult.

This figure shows a hypothetical failure histogram with frequency on the X axis and the number of failures on the Y axis. The histogram clearly shows that the target frequency (highlighted with the vertical bar) could be raised about 15 percent before hitting the point of diminishing returns. The shaded area represents everything beyond the "wall."



The "Wall": impossible to find without a complete, accurate model.

Our toolset extracts parasitics at each level of design hierarchy, providing efficient management of the large number of RC elements in the full design. Because our RC data is hierarchical, single RC networks are often split across multiple levels of hierarchy. For example, feedthroughs occur when a global-routed signal makes use of metal placed inside a circuit block. Frequently, a long wire will separate the driving transistor from the port of the block, creating a large RC delay at the block port. Since an RC delay is highly affected by the network's environment, most notably the driver strength and the receiver capacitance, our approach analyzed the entire network as a single unit to obtain accurate results.

Any approach to RC simulation must include some form of node foliation. Node foliation replaces the original "logical" node (as would appear in a schematic) with a network of resistors, capacitors, and artificially created and named

nodes. These nodes represent all of the internal points of the RC network, as well as differentiate each of the termination points (see Figure 1). The development of new tools for formatting and analyzing complex network connectivity enabled us to efficiently manage large netlists as the design evolved.

Connecting the ports Very often in custom designs, a circuit block will have multiple physical ports for a given "logical" port. In many cases, these ports are separated by significant global RC networks that require accurate modeling.

Connecting circuit-block timing specifications defined with logical ports to multiple physical block ports creates an interconnect modeling problem. In this case, there are at least three possible ways to model the connections, each with disadvantages that introduce inaccuracy. The physical ports may be shorted together and connected to the logical port, providing a simple solution but ignoring the global route resistance separating the physical ports. Instead, the logical port may be connected to the most critical physical port. However, it may be difficult to identify the critical port on a network connected to multiple drivers and receivers. Another alternative is to connect the logical port to the middle of a network, modeling the internal block connectivity to the physical ports.

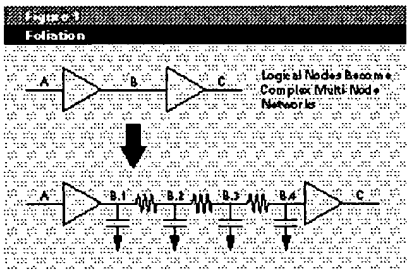


Figure 1. RC simulation requires foliation, in which a complex network of resistors, capacitors, and artificial nodes (created or "foliated" artificially) replace a "logical" node.

A more optimal general solution is to provide multiple circuit-block timing specifications for the multiple physical ports and connect them appropriately to the global routing.

Black boxes Our early global timing analysis used a gate-based static timing analyzer, which also read "black box" timing specifications. The "black box" timing specifications modeled the full-custom block designs based upon either designer's budgets, estimates, or data drawn from Spice simulation. The final PA-8000 model contained a set of approximately 80 major circuit-block timing

specifications. Paired with each major specification was another file containing RC networks, which modeled feedthroughs and long ported wires, and resolved multiple physical port connections.

Interconnect delays were precalculated by a network analyzer that combined RC data with driver strength and port capacitance information and generated a report of point-to-point delays.

The "black box" circuit-block specifications contained setup times, clock-to-out delays, combinational delays, and port capacitances for each logical port. These specs abstracted away any internal structures. The clock-to-out and combinational delays were modeled with two coefficient equations consisting of constant and load-dependent delay terms.

Strong points This early methodology displayed significant strengths. For example, using extracted parasitic data improved the RC delay calculation accuracy, particularly for complex RC networks with multiple branches and destinations. Such cases are not handled well by methodologies relying on estimated or lumped resistances and capacitances.

The early methodology excelled as a budgeting and communication tool. All circuit-block specifications and timing assumptions for each global signal were crosschecked, including the RC delays of the global route. The timing model provided a tracking mechanism and central database for global signal timing.

Our experience also identified several issues not adequately addressed by our early methodology. First, the large amount of budgeted and estimated data contained in the circuit-block specifications was time consuming to generate, verify, and keep current. Estimated data was often over worst-cased, skewing the position of the "wall" on the frequency histogram (see "Finding the Wall"). Second, our toolset was stressed by our large design, resulting in longer than desired loop times. Third, our analysis tools did not take full and efficient advantage of our design hierarchy. This limitation contributed significantly to our decision to develop a new methodology based on hierarchical analysis tools.

Finally, the problem of connecting single logical circuit-block specifications to multiple physical-block ports remained. Resolving each case manually added processing time and increased loop cycle times. We needed a general,

efficiently automated, and accurate solution integrated with a more-comprehensive, hierarchical timing methodology.

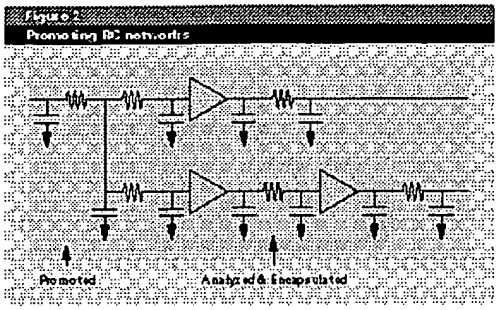


Figure 2. Ported RC networks are pulled out of the netlist for a child block and are moved up, or "promoted," to the next level of the hierarchy.

A new methodology At first tape release, the global timing team set out to address the limitations of our early timing approach while building on its strengths. As with our pre-silicon approach, we opted for static timing analysis to achieve complete path coverage. To avoid the problems associated with estimated timing specifications, we required a static timing analyzer capable of analyzing our custom designs at the transistor level, as well as at the gate level for library based designs. Early floorplanning still requires support for black-box and large memory structure models to reduce capacity limitations. To further improve efficiency, we decided to automate promotion of block-ported RC networks to higher levels of the hierarchy.

Our early timing methodology was limited to one level of hierarchy, forcing us to flatten our database before running the static timing analyzer, resulting in a large monolithic data set that slowed analysis. In addition, low-level design issues involving tightly coupled blocks were often identified by the global timing model, stealing post-processing bandwidth from the team and delaying feedback to the designers of the low-level block. Clearly, we wanted a flexible methodology to partition the hierarchy as needed and seamlessly integrate the block-level analysis into the global timing model.

Choosing an analyzer Central to achieving these goals was selecting a static timing analyzer capable of understanding our full-custom design styles and encapsulating them for global analysis. Of the commercial tools available, we opted for PathMill, from EPIC Design Technology Inc. (Sunnyvale, CA) for a number of reasons:

- PathMill analyzes high-performance circuit design styles, such as transparent latches, dynamic logic,

pseudo-NMOS, and gated clocks. Nearly all of our custom techniques either fall into one these categories or require some minor work-arounds.

- PathMill handles RC parasitic networks. Our tools are well-suited to generating netlists containing RC parasitics, so there is no need to calculate and backannotate RC delays.
- PathMill generates an abstraction of a block, called a gray box, which contains only the worst-case timing arcs between latches and ports. Using a gray box for each major block in a full-chip model reduces the amount of data for simulation.
- PathMill models may contain an integration of gray boxes, transistors, and RC parasitics. This flexibility provides an elegant structure for timing verification of hierarchical designs.

By creating and analyzing hierarchical timing models, PathMill not only reduces capacity requirements, it also enables us to iterate between design and analysis of tightly coupled blocks independent of the higher level timing model.

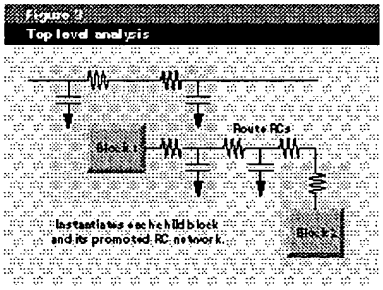


Figure 3. For analysis at the top level of the hierarchy, each child block and its promoted RC network is instantiated.

Data flow The data flow in this timing methodology is bidirectional. Detailed timing information from low-level blocks is pushed upward, while context information from the top level is pushed down. Low-level blocks are simulated and analyzed with PathMill before generation of gray box models, which are incorporated into a the top-level timing model. Block context information is determined at the top level and returned for the next iteration of lower level block simulation and gray box generation.

For tightly coupled blocks, we introduced a level of hierarchy called a minichip. At this level, the gray boxes of child blocks are instantiated along with any transistors and RC parasitics that were not abstracted at the lower levels. As in the block analysis, a minichip gray box is generated

and submitted for use in the top-level timing model.

The top-level netlist contains a mixture of RC parasitics from the global route; transistors for simple structures, such as signal repeaters; and gray boxes for top-level blocks and minichips.

When simulating the top-level model, PathMill generates context files for each block and minichip. These files contain loading information, input signal arrival times, and output signal timing requirements. This information improves the driver and receiver gray box characterization and communicates port timing to the block designer during low-level block analysis.

While building the PathMill netlist for a lower level block, RC networks based on parasitic extraction are generated to connect the block ports to the internal transistor circuits. Because delays through these RC networks are difficult to characterize until the complete network is present, ported RC networks are promoted to the higher level model via an automated process.

Consider the example shown in Figure 2. Before applying PathMill analysis to the block, the ported RC networks are removed from the netlist and promoted to the next level of hierarchy. PathMill encapsulates only the shaded portion into a gray box.

Minichips use the same RC promotion process. Full RC networks are assembled at the appropriate level of hierarchy, solving a host of problems associated with feed-throughs, long ported wires, and multiple ported signals.

The top-level netlist instantiates the gray boxes and RC networks for all top-level blocks and minichips (see Figure 3). Signal repeaters and other simple blocks may remain in transistor form and are not abstracted into gray boxes. At this level, the model contains a set of all worst-case timing arcs represented in each low-level block gray box and a complete RC network for each global routed signal, including the promoted lower level RC networks.

In summary This methodology provides a more comprehensive timing model where all speed paths are visible and reported with high accuracy. The path histograms correlated well with manufactured parts and predicted failure frequencies within 10 percent of silicon measurements. Higher accuracy translates into improved ability to identify the "wall," or point of diminishing

returns. This type of information is invaluable for selecting product frequencies, scoping follow-on projects, and identifying opportunities to increase performance and yield.

Using PathMill, we generated circuit-block timing specifications directly from the transistor-level analysis, making use of our hierarchical RC extraction toolset. Combining those specs, our RC promotion solution seamlessly integrates block and global timing, greatly increasing the accuracy and completeness of the entire process. The methodology also allows us to define minichips wherever their use was most productive.

These gains were accomplished while reducing the amount of handwork required to generate block-timing specifications and consolidate them into the global timing model.

By smoothing the path from block to global timing and dividing the hierarchy appropriately, we will be able to provide global timing feedback earlier and more often. This ability translates directly into faster time to market.

This methodology will continue to be refined. One of the biggest issues is the large amount of resource consumed. For the post-silicon analysis of the PA-8000, we generated approximately 50 Gbytes of data. More importantly, developing the methodology and completing the analysis required about ten engineers for six months. However, we believe the engineering requirements will be considerably lower as these processes become part of the incremental development and analysis of each circuit block.

This methodology proved its usefulness by identifying several timing paths that were not optimized during product development and would have been more costly to identify during silicon characterization. Due to its success, the methodology will be used on all of our current development projects.

Clay McDonald, Tom Indermaur, and Mike Buckley are design engineers at Hewlett-Packard Co. (Fort Collins, CO).

To voice an opinion on this or any *Integrated System Design* article, please e-mail your message to *michael@asic.com.*

[Articles from Integrated System Design Magazine] [ICs and uPs]
[Custom ICs and Programmable Logic] [Vendor Guide]
[Design and Development Tools] [Home]

For more information about isdmag.com e-mail cam@isdmag.com
For advertising information e-mail amstjohn@mfi.com
Comments on our editorial are welcome